IN THE CLAIMS:

Please cancel claims 23-26 without prejudice or disclaimer, and amend claims 27-28 as follows:

1-5. (Cancelled)

6. (Withdrawn) The semiconductor integrated circuit device as claimed in claim 1, wherein:

the connection wires are laid in at least one wiring layer; and

GND lines are laid between the connection wires or at least one GND layer is formed between the wiring layers.

7. (Withdrawn) The semiconductor integrated circuit device as claimed in claim 1, wherein an electrostatic discharge protection element is disposed in the vicinity of each said inspection pad.

8. (Withdrawn) A semiconductor integrated circuit package having leads on four sides, comprising:

a semiconductor integrated circuit device with bonding pads laid along one pair of opposite sides of the four sides; and

a table for supporting the semiconductor integrated circuit device,

wherein the bonding pads along the pair of opposite sides of the semiconductor integrated circuit device are connected with leads along the four sides of the package.

9. (Withdrawn) The package as claimed in claim 8, wherein the leads comprises:

first outer leads arranged along a first side of the package;

second outer leads arranged along a second side, perpendicular to the first side, of the package;

first inner leads corresponding to the first outer leads but being bent toward the second side; and

second inner leads corresponding to the second outer leads.

10. (Withdrawn) The package as claimed in claim 9, wherein the pads of the semiconductor integrated circuit device are arranged zigzag, and

bonding wires for connecting the pads of the semiconductor integrated circuit device to the tips of the inner leads have significantly the same length.

11. (Withdrawn) The package as claimed in claim 8, wherein an extension line of one side of the semiconductor integrated circuit device and an extension line of the closest side of the package are not parallel but intersect at a fixed angle.

12. (Withdrawn) The package as claimed in claim 11 wherein the fixed angle is 45°.

13. (Withdrawn) The semiconductor integrated circuit device as claimed in claim 1, wherein at least one electrostatic discharge protection element is provided for at least one of the inspection pads and the input/output buffer area.

14. (Withdrawn) The semiconductor integrated circuit device as claimed in claim 3, wherein said at least one connection wire laid inside the input/output buffer area circumvents or crosses over a package of the chip to extend from the bonding pad to the inspection pad.

15. (Withdrawn) The package as claimed in claim 8, where the leads constitute the table for-supporting.

16. (Withdrawn) The package as claimed in claim 8, wherein at least one electrostatic discharge protection element is provided for at least one of the pads.

17. (Withdrawn) The package as claimed in claim 9, wherein at least one of the second inner leads have tips arranged zigzag with respect to tips of the first inner leads.

18. (Withdrawn) The package as claimed in claim 9, wherein the second inner leads are connected to the second outer leads via wires outside of the semiconductor integrated circuit device and inside the package.

19. (Withdrawn) The package as claimed in claim 9, wherein each of the bonding pads is either connected to the inner leads with bonding wires, and the bonding wires are laid outside an input/output buffer area of the chip.

20. (Withdrawn) A semiconductor integrated circuit device, comprising:

a plurality bonding pads arranged along at least one side of a least one semiconductor chip embedded in the semiconductor integrated circuit device;

at least one inspection pad on another side of the semiconductor chip; and

a corresponding connection wire for each of said bonding pads for connecting said each bonding pad with the inspection pad,

wherein at least one of the bonding pads, the inspection pads and the connection wire is to be removed from the device when the device is cut off from a wafer.

21-26. (Cancelled)

27. (Currently Amended) A semiconductor integrated circuit device comprising:

a semiconductor chip embedded in the semiconductor integrated circuit device, the semiconductor chip comprising:

a first bonding pad arranged on a first side of the semiconductor chip;

a second bonding pad arranged on a second side of the semiconductor chip;

a first input and output buffer and a second input and output buffer which are coupled to the first and second bonding pads respectively;

a first inspection pad; [[and]]

a first connecting wire which is laid outside an area where the first and second input and output buffers are arranged and which connects the second bonding pad to the first inspection pad[[,]];

a plurality of other first bonding pads arranged on the first side of the semiconductor chip;

a plurality of other second bonding pads arranged on the second side of the semiconductor chip;

a plurality of other first connection wires; and

a plurality of other first inspection pads arranged on the first side of the semiconductor chip, each of the plurality of the inspection pads connected to the corresponding second bonding pads,

wherein the first inspection pad is arranged on the first side of the semiconductor chip, and

wherein each of the plurality of the first connection wires has an identical length.

28. (Currently Amended) [[The]] A semiconductor integrated circuit device ~~according to claim 23, further~~ comprising:

a semiconductor chip embedded in the semiconductor integrated circuit device, the semiconductor chip comprising:

a first bonding pad arranged on a first side of the semiconductor chip;

a second bonding pad arranged on a second side of the semiconductor chip;

a first input and output buffer and a second input and output buffer which are coupled to the first and second bonding pads respectively;

a first inspection pad;

a first connecting wire which is laid outside an area where the first and second input and output buffers are arranged and which connects the second bonding pad to the first inspection pad;

a third bonding pad arranged on a third side of the semiconductor chip, the third side facing the first side;

a fourth bonding pad arranged on the second side of the semiconductor chip;

a third input and output buffer and a fourth input and output buffer which are coupled to the third and fourth bonding pads respectively;

a second inspection pad; and

a second connection wire which is laid outside an area where the third and fourth input and output buffers are arranged and which connects the fourth bonding pad to the second inspection pad,

wherein the first inspection pad is arranged on the first side of the semiconductor chip and only connected to one bonding pad on the second side of the semiconductor chip such that the second bonding pad on the second side and

the first bonding pad on the first side are set to be tested concurrently through respectively probing the first inspection pad and the first bonding pad on the first side, and

wherein the second inspection pad is arranged on the third side of the semiconductor chip and only connected to one bonding pad on the second side of the semiconductor chip such that the fourth bonding pad on the second side and the third bonding pad on the third side are set to be tested concurrently through respectively probing the second inspection pad and the third bonding pad on the third side.